AMENDMENT TO THE SPECIFICATION

Please add a paragraph before the paragraph that currently begins at page 3 line 15 as follows:

FIG. 9 illustrates a machine readable medium that can be read by a computer.

Please amend the paragraph that begins at page 4, line 18 as follows:

In determining delay times of an integrated circuit, the integrated circuit may be broken down hierarchically into integrated circuit subsets (or design blocks). In order to understand the timing delays of an entire integrated circuit, the delay time through each integrated circuit subset in addition to the input capacitance and the setup/hold times of circuit blocks can be expressed as a function of various operating parameters such as metallization resistance and capacitance (i.e. Rint and Cint, respectively), power supply voltage (i.e. Vdd), process (i.e. transistor performance), and temperature. Therefore, if the sensitivities of delay time, input capacitance, and setup/hold time are characterized in terms of these operating parameters, the timing delay of the integrated circuit and its subsets can better be understood and modeled.

Please amend the paragraph that begins at page 5, line 4 as follows:

FIG. 2, for example, illustrates a model of a design block within an integrated circuit according to one embodiment of the present invention. Unlike the model of FIG. 1, the model of FIG. 2 includes additional parameters such as metallization resistance (Rint) and capacitance (Cint) in addition to Tx (input edge rate or transition time) and Cl. As discussed above, an integrated circuit may be broken down hierarchically into subset blocks. These blocks may each include multiple blocks down to a single component level or be a combination of many components such as an adder, multiplexer, cache, etc. Therefore, one example of an integrated circuit that may be found in the block of FIG. 2 is illustrated in FIG. 3. That is, there may be multiple components, illustrated here as inverters where the inverters may be any single component or collection of components that are coupled to each other by internal metal lines. Each of these internal metal lines has resistive and capacitive components that affect delay through the block. Also, there is metal lying at the output stage, illustrated in FIG. 3 at the output of the last inverter, which is coupled to the capacitive load. This metallization at the output also affects delay through the block of FIG. 3 and can be taken into consideration. The block of FIG. 3 can also be thought of as comprising three separate blocks, each of them including a single inverter and an output metal line having metallization RC components. Therefore, as used herein, Rint and Cint refer to the metallization RC, respectively. Note that metallization RC can also be referred to as internal RC (internal resistance / internal capacitance) or distributed RC (distributed resistance / distributed capacitance).

Please amend Equation 3 on page 7, lines 5-7 as follows:

$$\text{Delay} = K0 \cdot Tx^{-0.5} + K1 \cdot Tx + K2 \cdot Cl^{cl\_tx} \cdot Tx + K3 \cdot Cl^{cl\_exp} + K4 \cdot Cl + K5 + K6 \cdot Rint \cdot Cl + K7 \cdot Rint \cdot Cint + K8 \cdot Cint + K9 \cdot Cint^{cint\_exp} + K10 \cdot \sout{Cint^{eint\_exp} \cdot TX} \; \underline{K10 \cdot Cint^{cint\_tx} \; TX}$$

Please amend the paragraph that begins at page 12, line 24 and continues to page 13, line 6 as follows:

The term corresponding to K9 reflects the variance in the internal metallization capacitance and how this affects the perceived input capacitance of the circuit block. The constant K14 represents a transistor term. That is, if it is assumed within the circuit block that the metallization resistance ~~resistant~~ and capacitance is negligible, then the K14 term corresponds to the input capacitance of the transistor itself. Therefore, the K14 constant is modulated by the remaining terms in the equation as the operating points (metallization RC, process, Vdd, temperature, etc.) vary.

Please amend the paragraph that begins at page 27, line 1 as follows:

The various methods and techniques described herein such as, for example, the flow of FIG. 8, the derivation of the constants and exponents, the timing analysis, etc. may be implemented in software executing on a processor. Such software is stored in a computer readable medium (i.e. a machine readable medium), and the software includes a plurality of instructions that, when executed, cause the processor to perform the functions included in the method or technique. FIG. 9 shows machine readable medium 901 that is able to be read by computer 902. The processor is operably coupled to the computer readable medium and retrieves the plurality of instructions for execution. Such software may be embodied on one or more of computer hard disks, floppy disks, 3.5" disks, computer storage tapes, magnetic drums, static random access memory (SRAM) cells, dynamic random access memory (DRAM) cells, electrically erasable (EEPROM, EPROM, flash) cells, nonvolatile cells, ferroelectric or ferromagnetic memory, compact disks (CDs), laser disks, optical disks, and any like computer readable media.